

## AN6023

**Associated Project:** No  
**Associated Part Family:** nvSRAMs  
**Software Version:** None  
**Associated Application Notes:** None

### Application Note Abstract

This application note describes the nvSRAM basic operations. The 4 Mbit nvSRAM in 0.13  $\mu\text{m}$  SONOS QuantumTrap™ technology is also discussed here. The same descriptions apply to other Cypress nvSRAM parts.

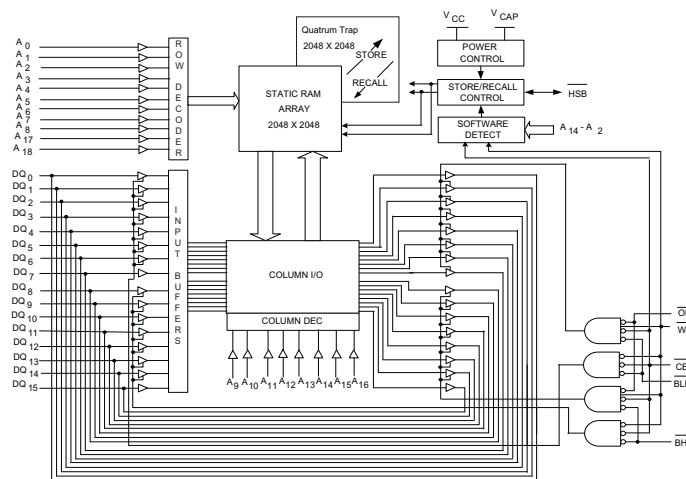
### Introduction

Memories that offer a combination of SRAM features along with nonvolatility have several advantages in a system. Cypress offers a family of high speed, high performance NonVolatile Static Random Access Memory (nvSRAM) products that combine the performance characteristics of a high speed SRAM with the reliability of QuantumTrap nonvolatile cell. The data is retained in the nonvolatile elements that are integrated with each SRAM cell. A STORE operation stores the SRAM data to the nonvolatile cells and a RECALL operation restores the nonvolatile data to the SRAM array.

Cypress nvSRAMs ensure secure storage of data by automatically storing the SRAM data to the nonvolatile cells on power down using charge from a capacitor. The nonvolatile Shadow EEPROM elements incorporate the SONOS QuantumTrap™ technology that guarantees nonvolatility for a minimum of 20 years at the maximum operating temperature<sup>[1]</sup>. Cypress nvSRAMs do not use batteries or any other energy sources to retain data.

**Note** The note references in this application note are listed in the Appendix [Differences in Features/Parameters Across Technology on page 4](#).

Figure 1. Logic Block Diagram



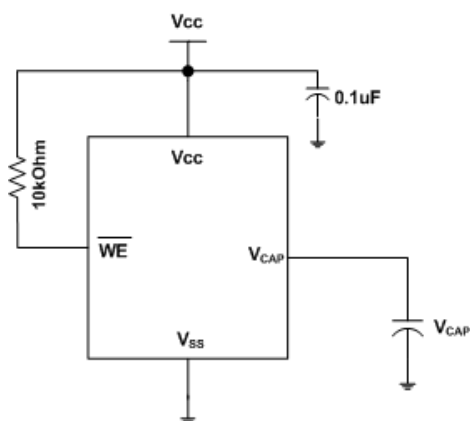
## Device Interface

The interface to the nvSRAM is identical to the high speed SRAM, except for a few extra pins exclusive to the device. [Figure 1 on page 1](#) shows the logic block diagram of a 4 Mbit (256K x 16) nvSRAM. The Address lines ( $A_0$ – $A_{18}$ ), the data lines ( $DQ_0$ – $DQ_{15}$ ), and the control lines ( $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  and  $\overline{WE}$ ) provide exactly the same interface as a high speed SRAM. For normal Read and Write operations, the nvSRAM is accessed in the same way as an SRAM, by appropriately toggling the three control signals CE (Chip Enable), OE (Output Enable) and WE (Write Enable).

The Power Control block is used to detect variations on the Power supply  $V_{CC}$  for triggering AutoStore™ operation. Software Detect Block is used for detecting address read sequences for STORE, RECALL and Enable/Disable AutoStore operations<sup>[2]</sup>. The STORE/RECALL Control block initiates STORE or RECALL operations, including Hardware Store operation using HSB pin.

The software sequences required to initiate nonvolatile operations use the standard SRAM control pins. As a result, very few hardware modifications are required to use nvSRAM in the place of standard SRAMs. The only external component required for nvSRAM operations is the capacitor connected to the  $V_{CAP}$  pin which is charged to the supply voltage<sup>[3]</sup> on power up. Charge from this capacitor is used to perform an AutoStore operation (transferring the contents of SRAM to nonvolatile elements on power down) operation. [Figure 2](#) shows the device configuration of nvSRAM in a system, including the capacitor connected to the  $V_{CAP}$  pin.

Figure 2. Device Configuration of nvSRAM <sup>[4]</sup>



## NonVolatile STORE Operation

A STORE operation is used to transfer the data in parallel from the SRAM to the nonvolatile Quantum Trap cells. For example, in a 4 Mbit nvSRAM, the data of all the 4M SRAM cells is stored to the 4M EEPROM elements simultaneously. This parallel transfer of data enables the entire SRAM array to be Stored in a maximum of 8 ms<sup>[5]</sup>. The nvSRAM STORE operation can be initiated in three ways: AutoStore, activated on device power down; Software Store, activated by a Software Read sequence; and Hardware Store, activated by the HSB pin.

During the STORE cycle, an erase of the previous nonvolatile data is first performed, followed by the programming of the nonvolatile elements. After a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

The HSB signal can be monitored by the system to detect if a STORE cycle is in progress. The busy status of nvSRAM is indicated by HSB being pulled LOW. To reduce unnecessary nonvolatile stores, AutoStore and hardware store operations are ignored unless at least one write operation has taken place since the most recent STORE or RECALL cycle. However, Software initiated STORE cycles are performed regardless of whether a write operation has taken place.

## AutoStore Operation

In AutoStore operation, data is automatically Stored into the EEPROM elements when the system Power supply  $V_{CC}$  drops below  $V_{SWITCH}$ <sup>[6]</sup>.

During normal operation, the device draws current from  $V_{CC}$  to charge the capacitor connected to the  $V_{CAP}$  pin. This stored charge is used by the chip to perform a single STORE operation. If the voltage on the  $V_{CC}$  pin drops below  $V_{SWITCH}$ , the part automatically disconnects the  $V_{CAP}$  pin from  $V_{CC}$  and a STORE operation is initiated with power provided by the  $V_{CAP}$  capacitor.

## Hardware STORE

The  $\overline{HSB}$  pin is used to request a hardware STORE cycle. When the  $\overline{HSB}$  pin is driven LOW by the controller, the nvSRAM conditionally initiates a STORE operation after  $t_{DELAY}$ <sup>[7]</sup>. However, a STORE cycle begins only if a write to the SRAM has taken place since the last STORE or RECALL cycle. The  $t_{DELAY}$  time allows completing any write operation that is in progress. The  $\overline{HSB}$  pin also acts as an open drain driver that is internally driven LOW to indicate a busy condition, when the STORE (initiated by any means) is in progress.

During any STORE operation, regardless of how it is initiated, the nvSRAM continues to drive the  $\overline{HSB}$  pin LOW, releasing it only when the STORE is complete. When the STORE operation is complete, the nvSRAM remains disabled until the  $\overline{HSB}$  pin returns HIGH. Leave the  $\overline{HSB}$  unconnected if it is not used.

## Software STORE

Data is transferred from the SRAM to the nonvolatile memory by a software address sequence. The software STORE cycle is initiated by executing sequential  $\overline{CE}$  or  $\overline{OE}$  controlled read cycles<sup>[8]</sup> from six specific address locations in exact order. During the STORE cycle, an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. After a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

## NonVolatile RECALL Operation

A RECALL operation copies data from EEPROM to SRAM, in parallel, at a maximum of 20 ms<sup>[9]</sup>. The RECALL cycle can be initiated by the following two methods:

### Power up RECALL

A request for power up RECALL is latched whenever the  $V_{CC}$  goes below  $V_{SWITCH}$ <sup>[10]</sup>. During power up, a RECALL operation is initiated when the  $V_{CC}$  crosses above  $V_{SWITCH}$ <sup>[10]</sup>. This ensures that the data that was written into SRAM before last power down is restored back on power up. Therefore, at power up, all Read and Write operation to the nvSRAM are blocked for the duration of the RECALL cycle.

### Software RECALL

A Software RECALL<sup>[11]</sup> operation is initiated in a similar manner as a Software STORE operation. This is done by reading a specific sequence of six address locations, with no access to other locations in between.

## The nvSRAM during NonVolatile Operations

During STORE and RECALL operations, the nvSRAM is not available to the system. All levels and transitions on the input pins are ignored and all data pins are tristated (except the HSB pin). After the nonvolatile cycle is completed, a READ or WRITE cycle can be initiated immediately by proper assertion of the control signals.

The  $\overline{HSB}$  pin is used to indicate when a nonvolatile STORE is in progress. This pin is internally driven LOW whenever a nonvolatile STORE is in progress.

If the  $\overline{HSB}$  pin is connected to any other device in the system, a pull up resistor to  $V_{CC}$  must be used on the HSB line. A weak internal pull up resistor keeps this pin HIGH, if a external pull up is not connected (connection optional). The value of the pull up resistor must be selected so that it does not overpower the internal pull down driver on HSB. Typically, a 10 K $\Omega$  pull up is sufficient.

## Protection Against Inadvertent STOREs

Cypress nvSRAM has several built in measures to prevent inadvertent STORE operations. The user initiated STORE operations are not allowed if  $V_{CC}$  is below  $V_{SWITCH}$ . This ensures that STOREs initiated by  $\overline{HSB}$  and software sequences are not started if  $V_{CC}$  is too low to allow successful completion.

Hardware STORE and AutoStore operations require that at least one WRITE operation takes place since the last nonvolatile operation. This feature ensures that a fluctuation on the supply line or noise on the HSB line does not initiate a second unnecessary STORE operation.

## Summary

Cypress nvSRAMs offer the functionality of fast Asynchronous SRAMs with the feature of nonvolatility. Cypress nvSRAMs retain data using integral QuantumTrap EEPROM providing high reliability. This eliminates the use of battery or any other source to back up data on power down. The nvSRAMs have the same Address, Data, and Control interface as an Asynchronous SRAM, thus simplifying interfacing and designing using the device.

## Appendix

Table 1. Differences in Features/Parameters Across Technology

Note Number <sup>a</sup>	Feature/Parameter		Technology		
			0.8 $\mu$	0.25 $\mu$	0.13 $\mu$
1	Data Retention		100 years at 125°C	20 years at 55°C	20 years at 85°C
2	AutoStore Enable/Disable		No	Yes	Yes
3	V <sub>CAP</sub> Voltage		V <sub>CC</sub>	5V	V <sub>CC</sub>
4	Device Configuration	Chip Power	V <sub>CAP</sub>	V <sub>CC</sub>	V <sub>CC</sub>
		Bypass Cap on	V <sub>CAP</sub>	V <sub>CC</sub>	V <sub>CC</sub>
5	STORE cycle duration	Non-RTC	10 ms	12.5 ms	8 ms
		RTC	-	15 ms	8 ms
6	V <sub>SWITCH</sub>	3V	2.7 to 2.95V	2.65V	2.65V
		5V	4.0 to 4.5V	-	4.4V
7	Time Allowed to Complete SRAM Write Cycle (t <sub>DELAY</sub> )		>1 $\mu$ s	1 to 70 $\mu$ s	1 to 70 $\mu$ s <sup>[b]</sup>
					25 ns
8	Read cycles for Software sequence generation		CE controlled; OE Don't Care	CE or OE controlled (Both must go LOW)	CE or OE controlled (Both must go LOW)
9	Power up RECALL (t <sub>HRECALL</sub> )	Non-RTC	550 $\mu$ s	20 ms	20 ms
		RTC	-	40 ms	20 ms
10	V <sub>CC</sub> level that will latch an automatic RECALL request		V <sub>CC</sub> < V <sub>RESET</sub>	V <sub>CC</sub> < V <sub>SWITCH</sub>	V <sub>CC</sub> < V <sub>SWITCH</sub>
11	Software RECALL (t <sub>RECALL</sub> )	Non-RTC	20 $\mu$ s	120 $\mu$ s	200 $\mu$ s
		RTC	-	170 $\mu$ s	200 $\mu$ s
12			CY14E256L/STK14C88 STK11C68 STK11C88 STK12C68 STK14C88-3 STK15C88 STK16C88 STK16C88-3 STK22C48	CY14B101L/STK14CA8 CY14B101K/STK17TA8 CY14B256L/STK14D88 CY14B256K/STK17T88	CY14B104L, CY14B104N CY14B108L, CY14B108N CY14B104K, CY14B104M CY14B10xLA, CY14B10xNA CY14B10xKA, CY14B10xMA

a. This table is intended to be illustrative. For more information, refer to individual data sheets.

b. t<sub>DELAY</sub> is 1 to 70us for CY14B104L, CY14B104N. For all the other parts in 0.13  $\mu$ , t<sub>DELAY</sub> is 25ns.

## Document History Page

**Document Title: NonVolatile SRAM (nvSRAM) Basics**

**Document Number: 001-14734**

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1778687	SHOR	11/28/2007	New application note.
*A	2662643	NXR	02/20/2009	Updated the content. Added Appendix to list the differences in Features/Parameters Across Technology. Changed title to "NonVolatile SRAM (nvSRAM) Basics".

In March of 2007, Cypress recataloged all of its Application Notes using a new documentation number and revision code. This new documentation number and revision code (001-14734, beginning with rev. \*\*), located in the footer of the document, will be used in all subsequent revisions.

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